

FEATURES

- E2-band coverage
- P1dB 24 dBm, OIP3 30dBm.
- Gain 17 dB
- Direct conversion or IF up-conversion
- Size: 12 x 15 x 3.75 mm (x, y, z)

DESCRIPTION

gMTX0017 is a surface-mount GaAs fully integrated transmitter SiP for the 71-76 GHz frequency band. The transmitter offers a wide IF bandwidth from DC to 10 GHz suitable for direct conversion or IF modulation/demodulation. The transmitter is highly linear with respect to IIP2/3. The package output has a WR-12 aperture for low-loss connection to a rectangular waveguide.

TYPICAL APPLICATIONS

- Point-to-point communication
- Instrumentation
- Active imaging
- General purpose

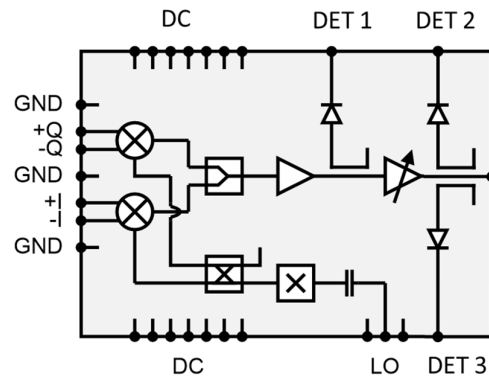


Figure 1. Circuit block diagram.

ELECTRICAL PERFORMANCE

Table 1. Electrical Performance. T_A=25°C, nominal bias

Parameter	Min	Typ	Max	Unit
RF frequency	81 (75)		86 (87)	GHz
IF frequency	DC		10	GHz
LO input frequency	13.5 (11.3) ¹		14.3 (14.7) ¹	GHz
LO input power		5		dBm
LO multiplication factor		6		
Max conversion gain		17		dB
Gain control range		25		dB
P _{1dB}		24		dBm
PSAT		26		dBm
OIP ₃		30		dBm
RF return loss		10		dB
IF return loss		10		dB
LO return loss		10		dB
Power consumption		2.8		W

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute maximum ratings

Parameter	
Gate-source voltage	-2 to +0.7 V
Drain-source voltage	4.5 V
Gate-drain breakdown voltage	8 V
Operating temperature	-40 to + 85°C
Storage temperature	-65 to +150°C

¹ X6 multiplier frequency extends beyond RF range

RECOMMENDED OPERATING CONDITIONS

Apply the gate (VG..) supplies first followed by the drain (VD..) supplies. Gate voltages are adjusted within the typical min/max range to obtain the specified drain currents. The drain currents are stated with all input signals off.

Table 3. Pin functions and electrical settings

Pin	Function	Bias settings (V/mA)			I/O	Sequence
		Min	Typ	Max		
1	NC					
2	NC					
3	NC					
4	VD2_VGA	3.2	3.3 / 400	3.4	I	2
5	VG2_VGA	-0.7	-0.5	-0.3	I	1
6	VG1_VGA	-0.7	-0.5	-0.3	I	1
7	VD1_VGA	3.2	3.3 / 275	3.4	I	2
8	VDET_1				I/O	
9	VREF_1				I/O	
10	VD_BUF	3.2	3.3 / 50	3.4	I	2
11	VG_BUF	-0.7	-0.5	-0.3	I	1
12	VG_MIX	-1.0	-0.8	-0.6	I	1
13	NC					
14	NC					
15	NC					
16	NC					
17	I+	Zo = 50Ω differential impedance, DC-coupled				
18	I-					
19	Q+	Zo = 50Ω differential impedance, DC-coupled				
20	Q-					
21	NC					
22	V-TEMP					
23	NC					
24	VG_AMP_X6	-0.65	-0.45	-0.25	I	1
25	VD_X2	3.2	3.3 / 108	3.4	I	2
26	VG_X2	-1.0	-0.8	-0.6	I	1
27	VD_X3	4.0	5.0 / 8	6.0	I	2
28	VG_X3	-0.95	-0.75	-0.55	I	1
29	LO	Zo = 50Ω, AC-coupled				
30	VREF_2				I/O	
31	VDET_2				I/O	
32	NC					

33	NC					
34	NC					
35	RF OUT (WR-12)					

MEASURED PERFORMANCE

Measurements have been performed at room temperature with typical bias settings if not specified otherwise.

Table 4. Test conditions

Input tone power	-8 dBm/tone
Two-tone frequency separation	50 MHz
Backside temperature	+25°C

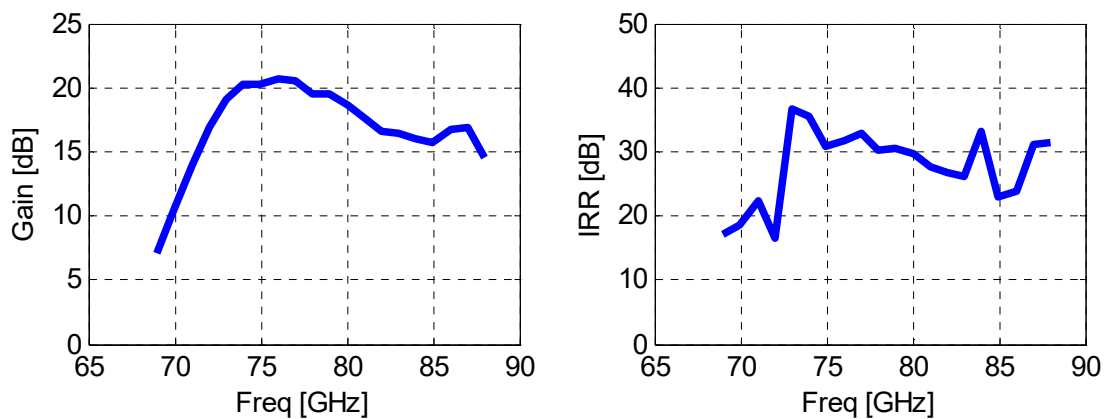


Figure 2. Gain (left) and image-reject-ratio (right) vs frequency.

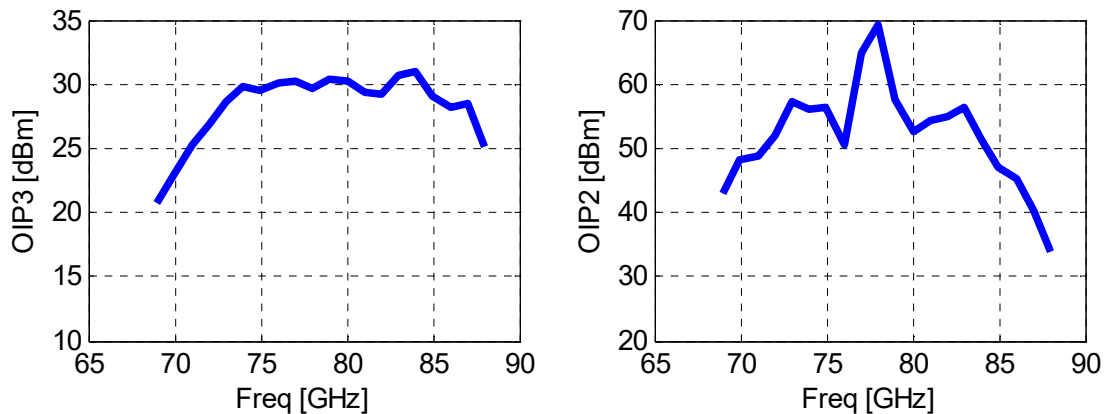


Figure 3. OIP3 (left) and OIP2 (right) vs frequency.

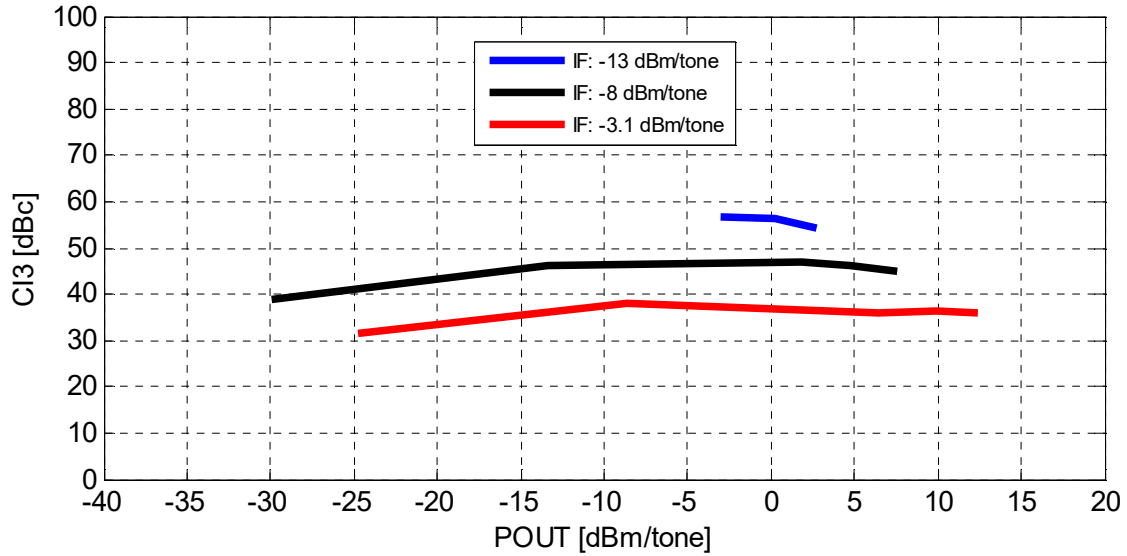


Figure 4. CI3 vs output power with the input power fixed at 83.5 GHz.

DETECTOR OPERATION

Detector 2 can be configured for RMS power or envelope detection. To compensate for thermal variation a reference is included on chip. Therefore, to get a temperature compensated output, take the difference of VREF and VDET using the recommended external detector circuit. Detector bias is applied through VDD and a pair of resistors with ideally identical value, 10k to 100k typical. We recommend selecting an operational amplifier with excellent input offset voltage performance, eg. Linear Technology LT1012.

Det 1 TBD

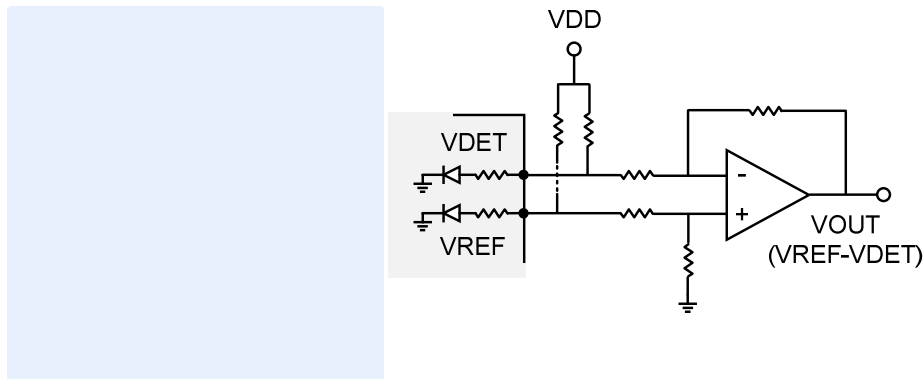


Figure 5. Detector output vs output power (left) and external detector circuit (right).

When configured for envelope detection it is necessary to keep transmission line lengths to a minimum and select external components with good RF performance to support signals with a wide bandwidth. This includes the bias-T, which can be as simple as a shunt resistor and a series capacitor connected to VDET. Bias current is regulated with the resistor and the envelope signal goes through the capacitor. Typical bias current is 1 mA. Input impedance at the pad of VDET is 200 Ohm. The reference is not required for envelope detection.

ASSEMBLY

The SMD assembly can be mounted as described by the EVB products as seen below
This product is available to customers as well.

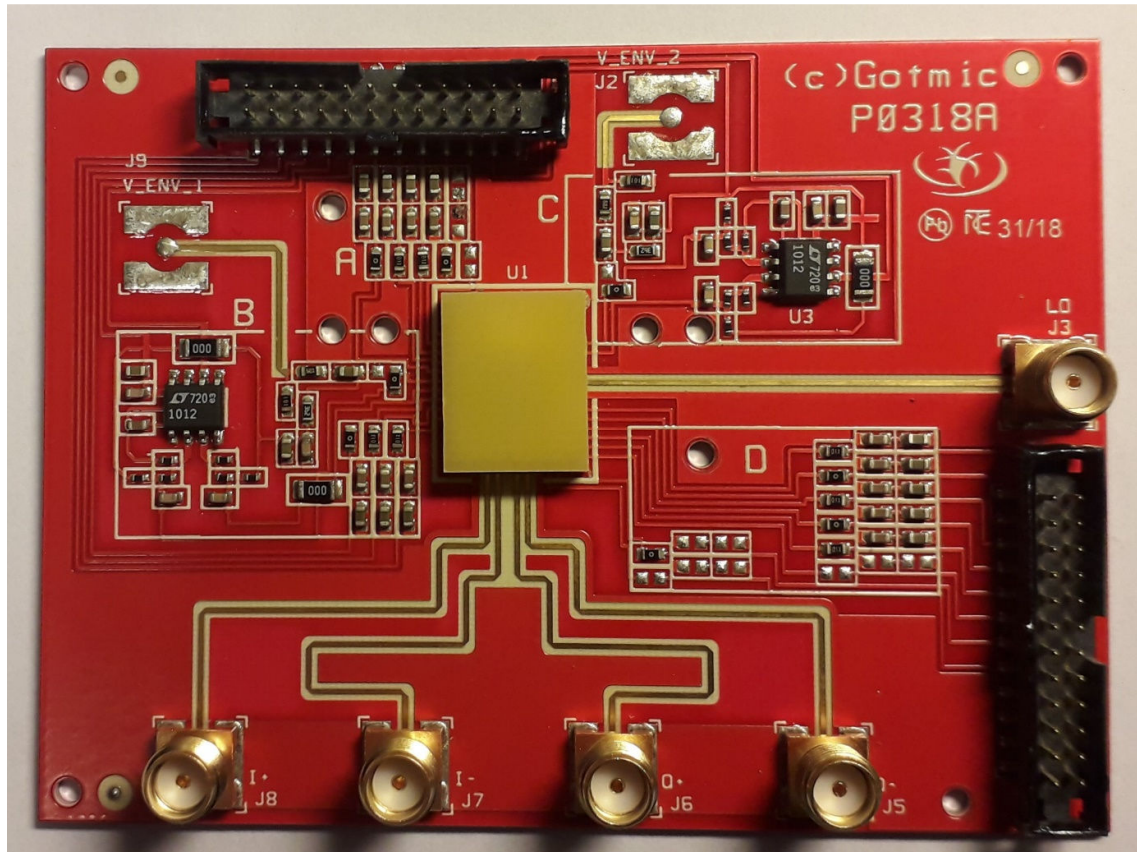


Figure 6. Photo EVB-gMTX0017

PIN CONFIGURATION

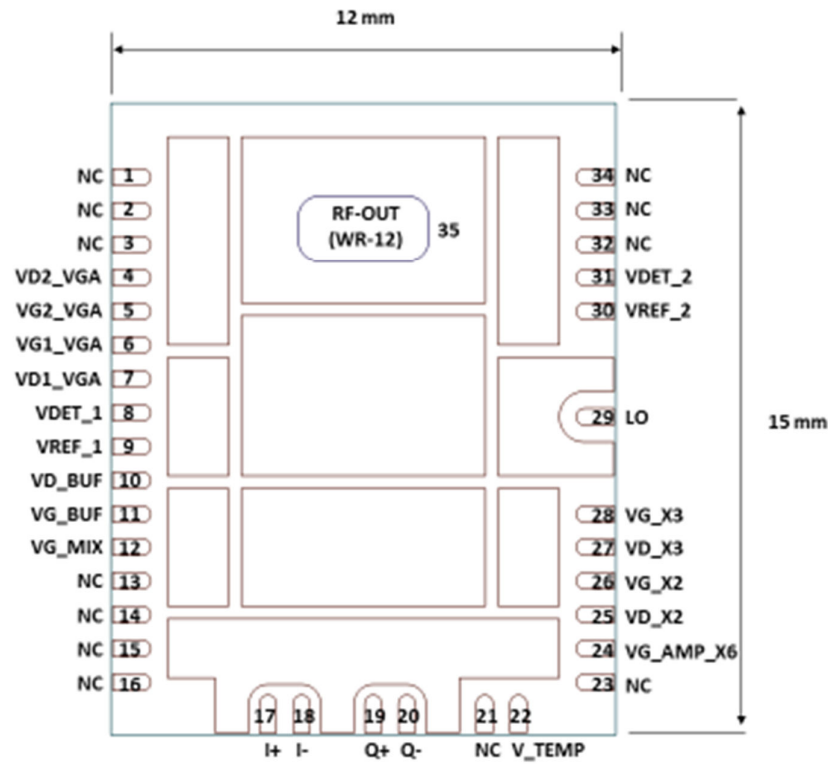


Figure 7. SMD pin configuration