FEATURES

- 92 - 100 GHz
- IIP2/3: 20/0 dBm
- Gain: 15 dB
- Direct conversion or IF down-conversion
- Size: 16 x 18 x 4 mm
- Evaluation board available

DESCRIPTION

gMRX0033 is a surface-mount GaAs receiver for the 92 - 100 GHz frequency band. The receiver offers a wide IF bandwidth from DC to 10 GHz suitable for direct conversion or IF modulation/demodulation. The package input features a WR-10 aperture for low-loss connection to a rectangular waveguide.

TYPICAL APPLICATIONS

- Point-to-point communication
- Radar and imaging
- Instrumentation
- Fiber over radio

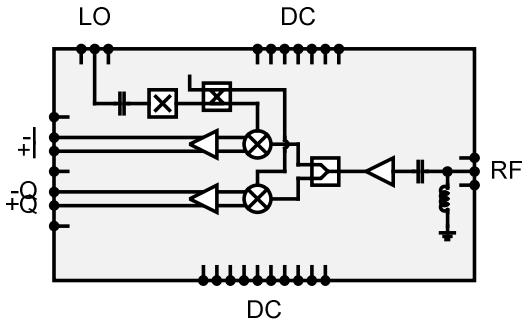

Figure 1. Circuit block diagram.

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ELECTRICAL PERFORMANCE

Table 1. Electrical Performance. T_A=25°C, nominal bias.

Parameter	Min	Typ	Max	Unit
RF frequency	92		100	GHz
IF frequency	DC		10	GHz
LO input frequency	11.5		12.5	GHz
LO input power		2		dBm
LO multiplication factor		8		
Conversion gain		15		dB
IIP2		20		dBm
IIP3		0		dBm
NF		6		dB
RF return loss		10		dB
IF return loss		10		dB
LO return loss		10		dB
Power consumption		1.4		W

Table 2. Absolute maximum ratings

Parameter	
Gate-source voltage	-2 to +0.7 V
Drain-source voltage	4.5 V
Gate-drain breakdown voltage	8 V
Operating temperature	-40 to + 85°C
Storage temperature	-65 to +150°C

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PIN CONFIGURATION AND BIAS

Always apply the gate supplies first followed by the drain supplies. It is recommended to initially set all gates to -1.6 V and adjust the gate supplies to obtain the specified drain currents. Read carefully the bias sequence for the IF low noise amplifier in ***. The typical gate voltage can vary by up to 0.2 V from what is noted. The drain currents are listed with all RF input signals off.
Note: Not connected (NC) pins are floating and must not be grounded.

Table 3. Pin functions and electrical settings

Pad No.	Reference	Supply (V)	Current (mA)	Function
1	NC			
2	NC			
3	NC			
4	VG_LNA	-0.5 (typ)		Bias
5	NC			
6	VD_LNA	1.5	60	Bias
7	VG_MIX	-0.8 (typ)		Bias
8	VI-_ADJ**	(-1) – (+1)	<10	Bias
9	VI+_ADJ**	(-1) – (+1)	<10	Bias
10	VQ-_ADJ**	(-1) – (+1)	<10	Bias
11	VQ+_ADJ**	(-1) – (+1)	<10	Bias
12	VD1_AMP***	7.0	55-65	Bias
13	VS_AMP***	-3.0	110-130	Bias
14	VG1_AMP***	-3.45 (typ)		Bias
15	VD2_AMP***	3.3	55-65	Bias
16	VG2_AMP***	-3.45 (typ)		Bias
17	Q+	Z0 = 100Ω differential impedance, DC-coupled		Output
18	Q-			Output
19	I+	Z0 = 100Ω differential impedance, DC-coupled		Output
20	I-			Output
21	NC			
22	VTEMP			Output
23	NC			
24	VG_AMP_X2	-0.5 (typ)	(78)	Bias
25	VD_AMP_X2	3.3	80 (78+2)	Bias
26	VG_X2	-0.9 (typ)	(2)	Bias
27	NC			
28	NC			
29	LO	Z0 = 50Ω, AC-coupled		LO
30-41	NC			
42	RF IN	WR-10		Input
43-54	GND			GND

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** Mixer offset adjustment (optional). Any small level differential common- or differential mode imbalance can be adjusted by tuning the I+_ADJ, I-_ADJ, Q+_ADJ and Q-_ADJ. If not used, leave open circuited.

*** Bias sequence for the integrated IF low noise amplifier is: 1) VG1_AMP, VG2_AMP, VS_AMP, VD1_AMP and 2) VD2_AMP. Depending on ac or dc coupled I+, I-, Q+ and Q- output ports, adjust VG1_AMP and VG2_amp until either the output voltage of I+,I-,Q+ and Q- ports become zero (dc coupled), or I+_ADJ, I-_ADJ, Q+_ADJ and Q-_ADJ adjust ports become zero (ac-coupled). Note that if the termination impedance is 50 Ω and the IF low noise amplifier is dc coupled, current will flow into the termination load unless the output voltage is zero. The sum of the currents from VD1_AMP and VD2_AMP should equal VS_AMP, and the voltage levels of the output ports I+, I-, Q+ and Q- (dc-coupled) or I+_ADJ, I-_ADJ, Q+_ADJ and Q-_ADJ ports (ac-coupled) are zero, then the IF low noise amplifier is biased correctly.

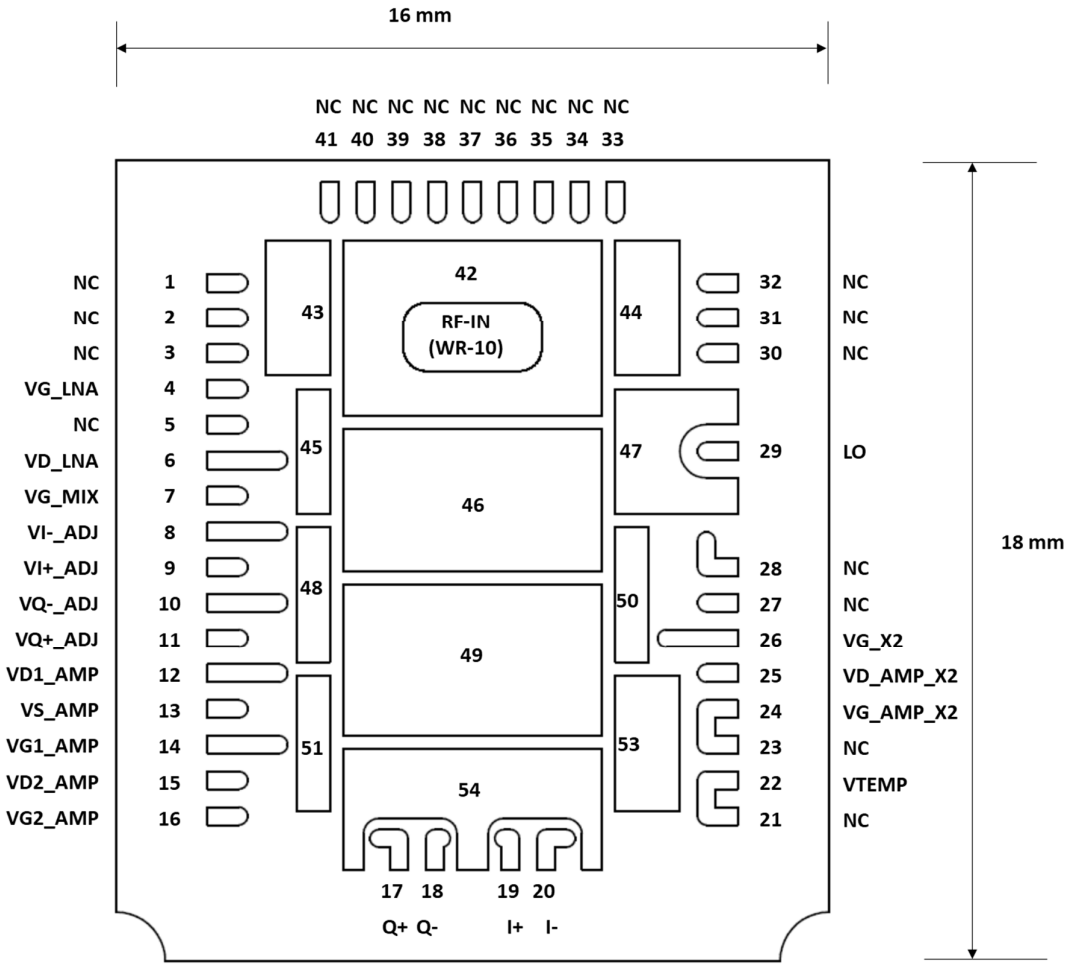

Figure 2. Pin configuration.

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