gMPA0035A
SMD E-band Power Amplifier
71-76 GHz (68-79 GHz)

Features

- SMD package (WR-12 interface)
- 71-76 GHz
- 28/29 dBm P1dB/PSAT
- 34 dBm OIP3
- 21 dB gain
- Integrated detector
- Nominal bias: 4.0 V and 1.3 A
- Size: 12 x 20 x 4 mm

Applications

- Point-to-point communication
- Radar and imaging
- Instrumentation
- Fiber over radio

Description

The gMPA0035A is a GaAs pHEMT four-stage power amplifier in a surface mount package optimized for 71-76 GHz. It has 21 dB gain and 34 dBm OIP3 making it ideal for long-range spectral efficient E-band point-to-point communication.

At a nominal bias of 4.0 V and 1.3 A the circuit dissipates 5.2 W and deliver 29 dBm saturated power at 12 % PAE.

A temperature compensated detector is available and can be configured for RMS power or envelope detection.

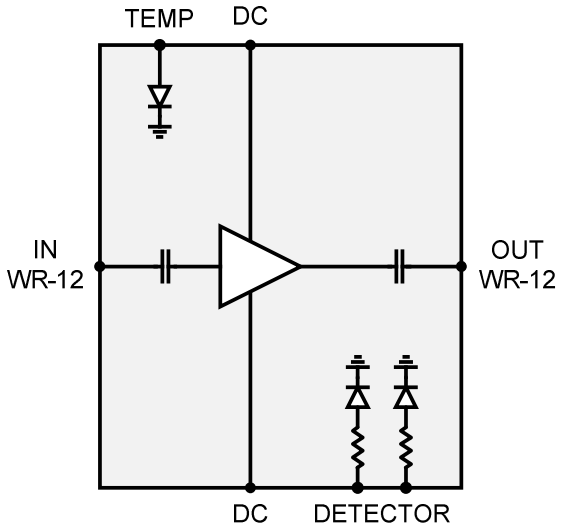

Figure 1. Circuit block diagram

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ELECTRICAL SPECIFICATIONS

Table 1. Electrical specifications, backside temperature +25 °C, nominal bias

Parameter		Min	Typ	Max	Unit
Frequency Range (performance)		71		76	GHz
Frequency Range (extended)		68		79	GHz
Gain			21		dB
Gain Temperature Slope			-0.05		dB/°C
OP1dB			28		dBm
PSAT (3 dB compression)			29		dBm
PAE at PSAT			12		%
OIP3			34		dBm
Input Return Loss			10		dB
Output Return Loss			10		dB
Detector Output at POUT *(VREF - VDET)*	-10 dBm		3		mV
	0 dBm		20		
	10 dBm		100		
	20 dBm		500		
	30 dBm		2000		
PDC (quiescent)	3.3 V / 1.3 A		4300		mW
	4.0 V / 1.3 A		5200		

Table 2. Absolute maximum ratings

Gate voltage (VG..)	-2.0 V
Drain voltage (VD..)	+4.5 V
Drain currents (*quiescent): VD (one-sided bias / two-sided bias)	 1560 mA / 1720 mA
VDET and VREF	50 uA
RF input power	+20 dBm
Junction temperature (1 million hours MTTF) *Thermal resistance (+85 °C backside temp)*	+150 °C *10 °C/W*
Operating temperature	-40 to +85 °C
Storage temperature	-65 to +150 °C

* Max rated drain current (quiescent bias) is limited by max junction temperature (at 4.0 V) and metal electro-migration. When operating the circuit near saturation the currents are allowed to increase beyond this limit except when applying bias from just one side.

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Pin Configuration and Bias

Always apply the gate supplies first followed by the drain supplies.

It is recommended to initially set the gate to -1.6 V and adjust the gate supply to achieve the specified total drain current of 1.3 A.

The typical gate voltage can vary by up to 0.2 V from what is noted.

The drain currents are listed with all RF input signals off.

Table 3. Pin configuration

Pad No.	Reference	Supply (V)	Current (mA)	Function
1-2	NC			
3-5	VD_A	4.0	650	Bias
6	NC			
7	VG	-0.5 (typ.)		Bias
8	NC			
9	V_TEMP	See temperature sensor		Temperature output
10-22	NC			
23	RF IN	WR-12		RF input
24-37	NC			
38-40	VD_B	4.0	650	Bias
41	VREF	See detector operation		Detector reference
42	VDET			Detector output
43-45	NC			
46	RF OUT	WR-12		RF output

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TYPICAL PERFORMANCE

Unless otherwise noted, all data presented has been obtained with a test-fixture, at room temperature and at nominal bias.

The two-tone RF input signal at -8 dBm/tone has a separation frequency of 50 MHz.

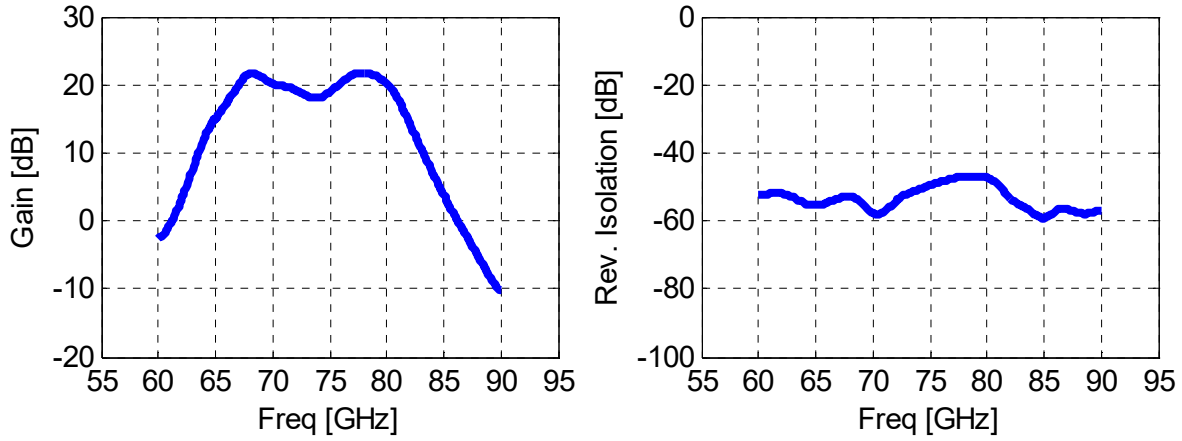

Figure 2. Gain (left) and reverse isolation (right)

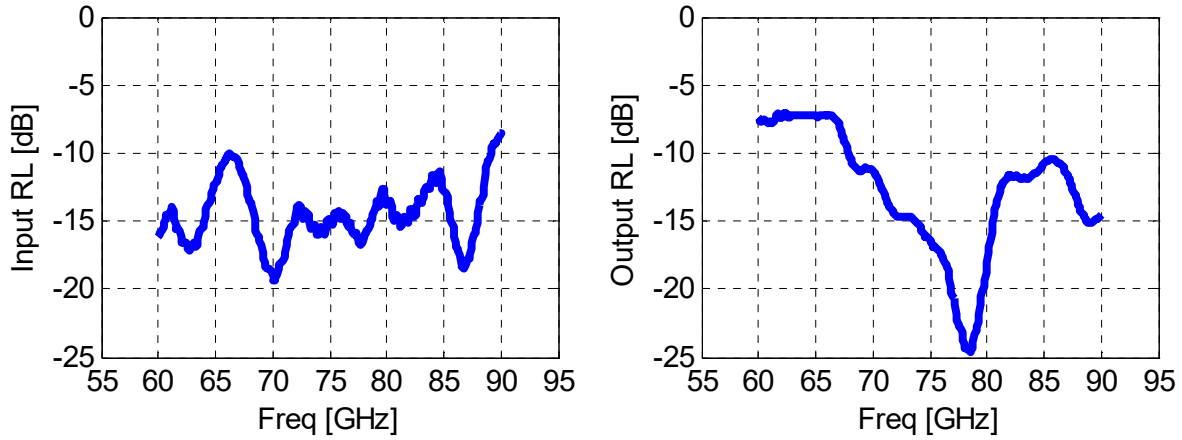

Figure 3. Input (left) and output return loss (right)

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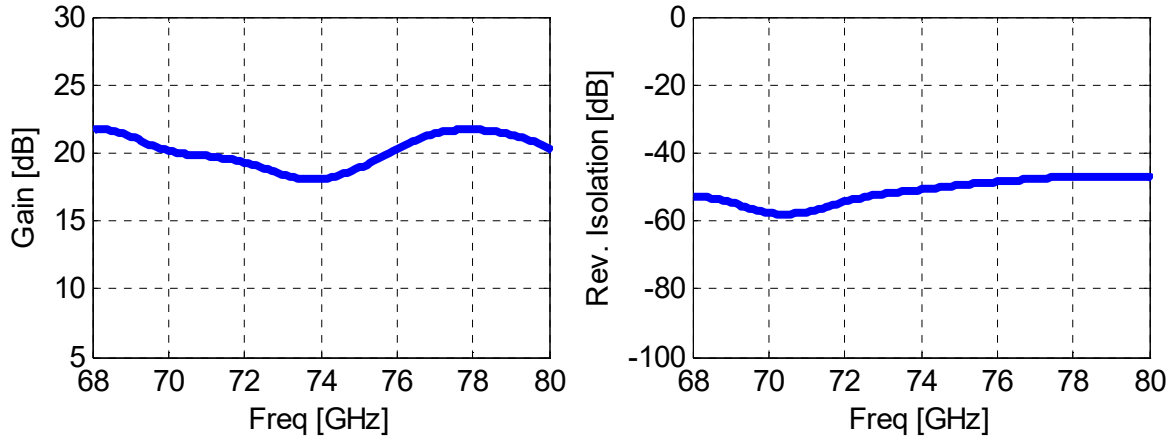

Figure 4. In-band gain (left) and reverse isolation (right)

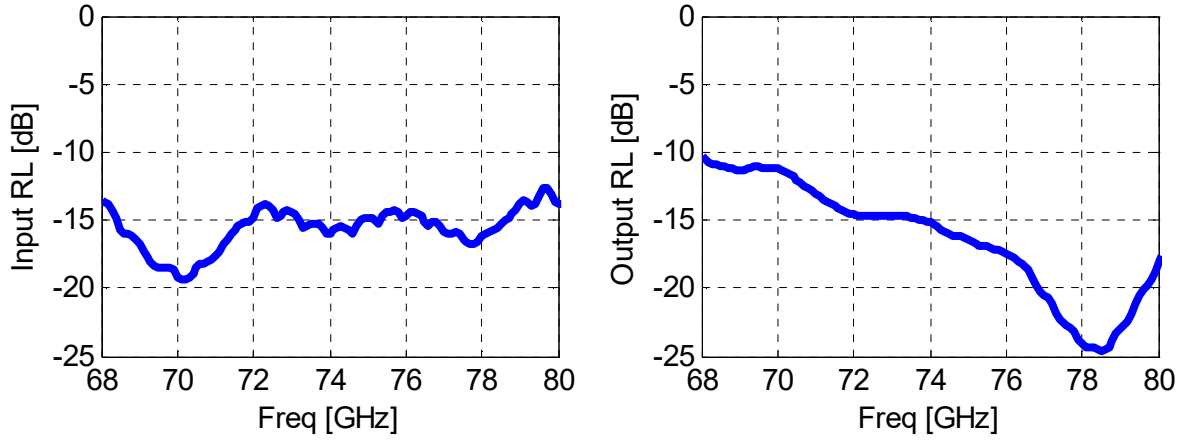

Figure 5. In-band input (left) and output return loss (right)

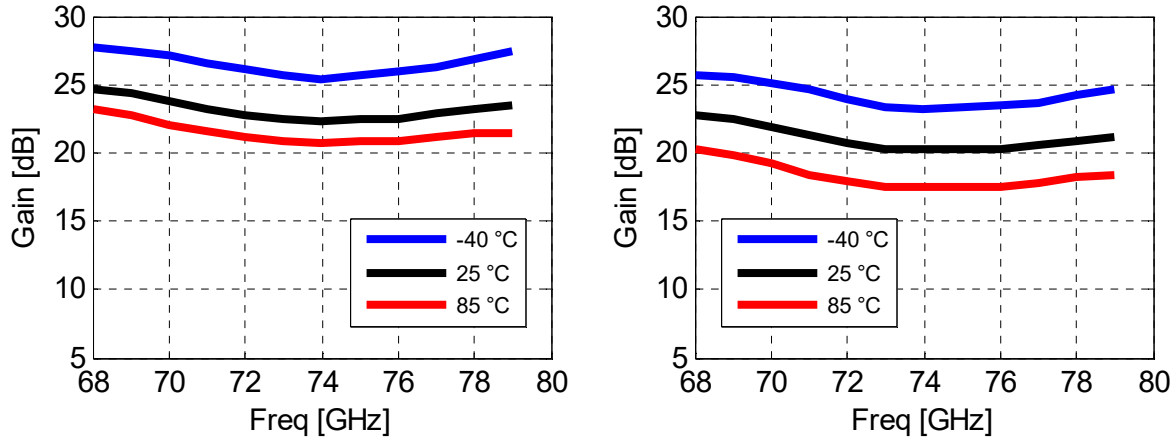

Figure 6. Gain at 3.3 V / 1.3 A (left) and 4.0 V / 1.3 A (right)

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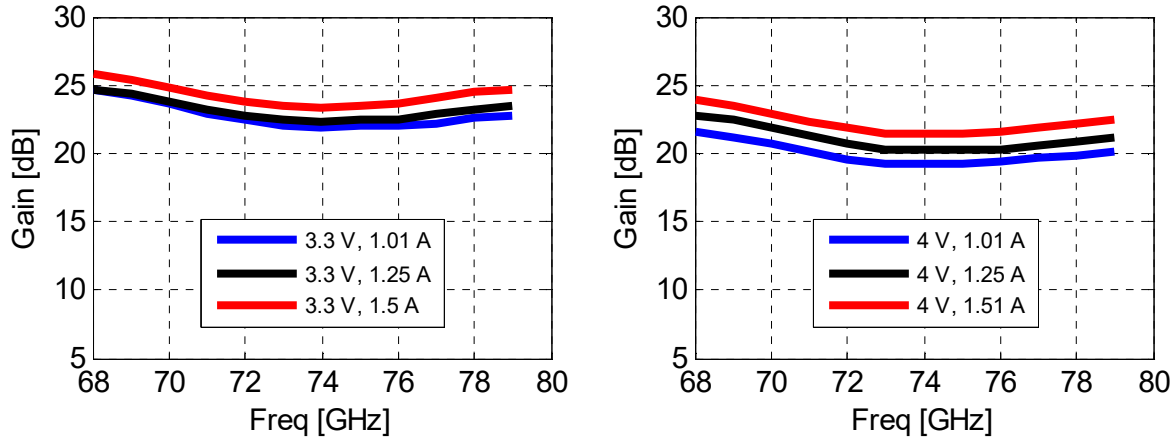

Figure 7. Gain at 3.3 V (left) and 4.0 V (right)

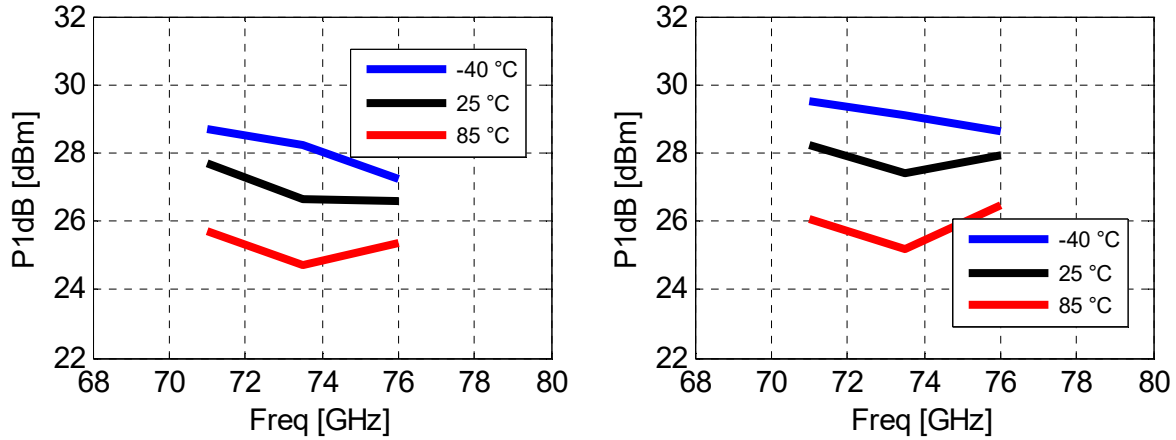

Figure 8. P1dB at 3.3 V / 1.3 A (left) and 4.0 V / 1.3 A (right)

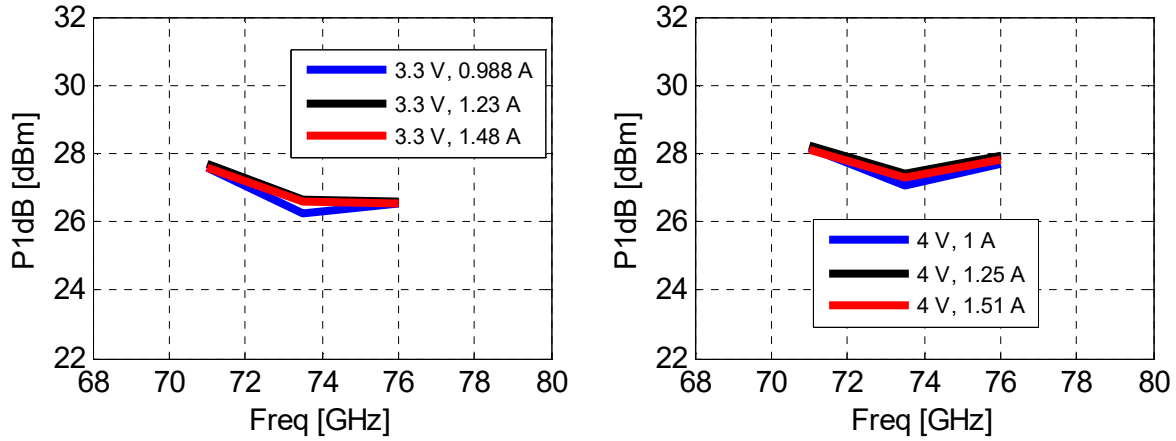

Figure 9. P1dB at 3.3 V (left) and 4.0 V (right)

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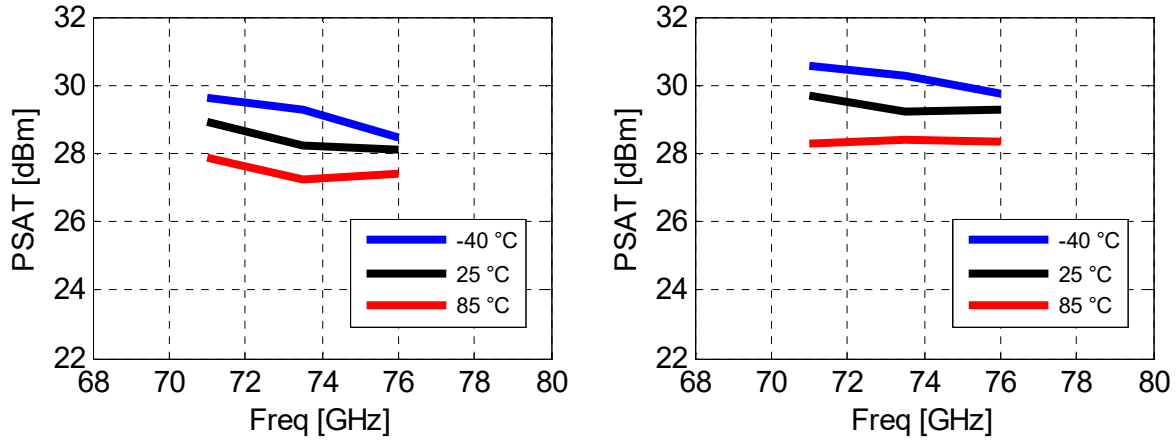

Figure 10. PSAT at 3.3 V / 1.3 A (left) and 4.0 V / 1.3 A (right)

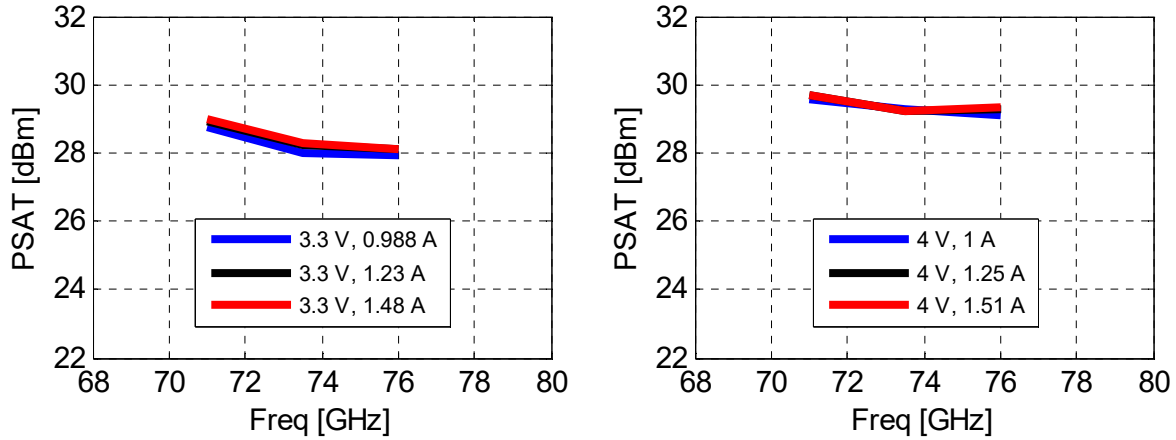

Figure 11. PSAT at 3.3 V (left) and 4.0 V (right)

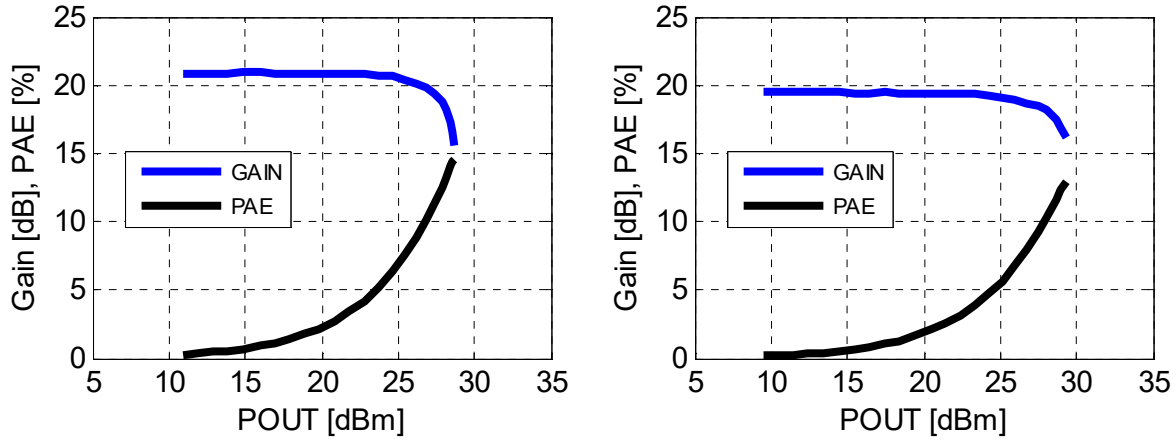

Figure 12. PAE at 3.3 V / 1.3 A (left) and 4.0 V / 1.3 A (right), 73.5 GHz

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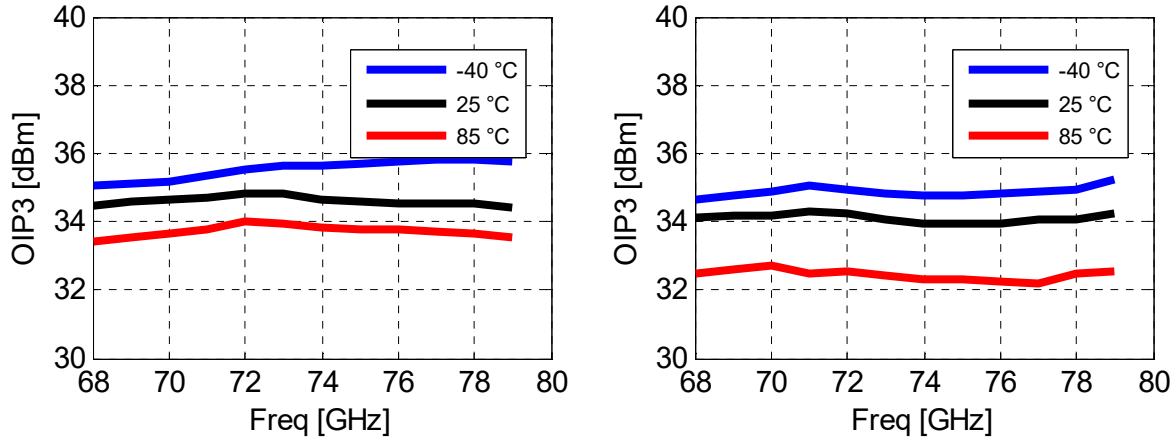

Figure 13. OIP3 at 3.3 V / 1.3 A (left) and 4.0 V / 1.3 A (right)

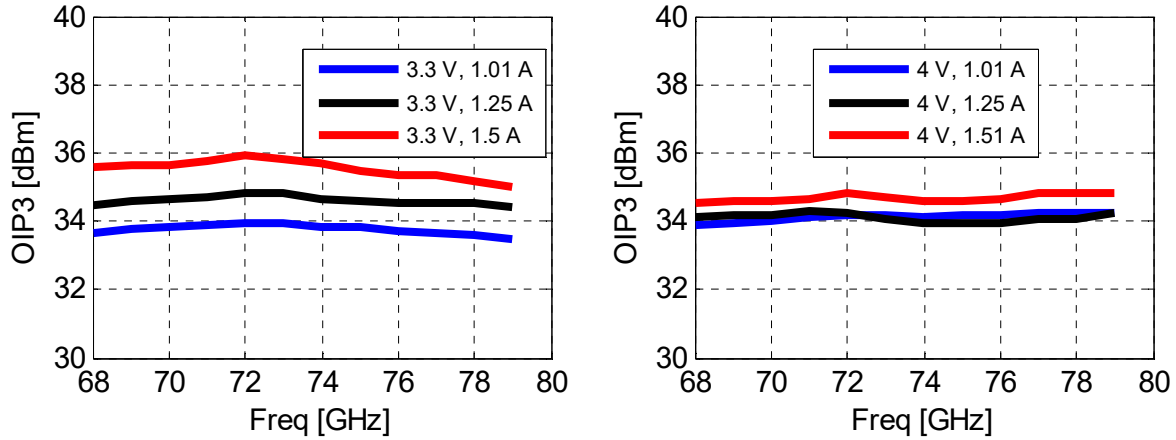

Figure 14. OIP3 at 3.3 V (left) and 4.0 V (right)

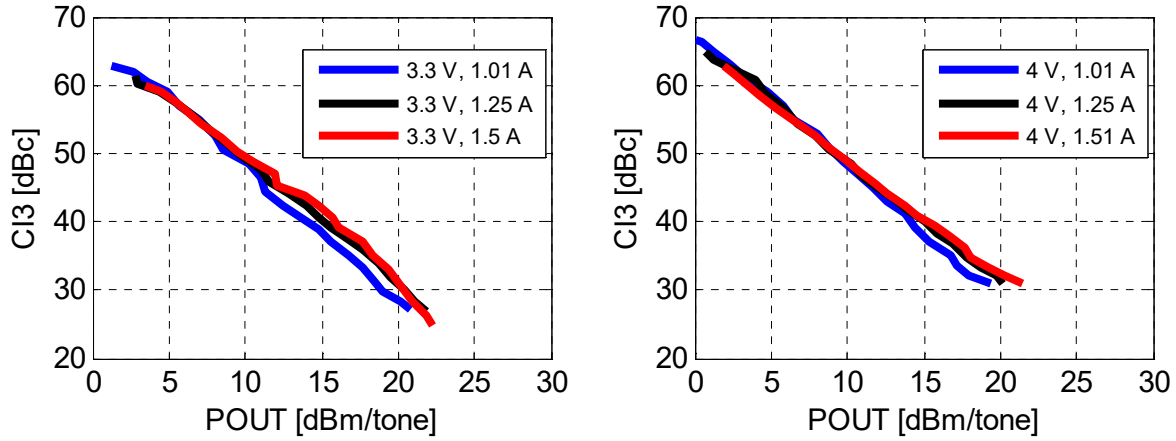

Figure 15. CI3 at 3.3 V (left) and 4.0 V (right), 73.5 GHz

Detector Operation

The detector can be configured for RMS power or envelope detection. Leave VREF and VDET as no-connect if not used.

To compensate for thermal variation, a reference is included on chip. Therefore, to get a temperature compensated output, take the difference of VREF and VDET using the recommended external detector circuit. Detector bias is applied through VDD and a pair of resistors, typically VDD is 5.0 V and R1-R2 is 100 kOhm. We recommend selecting an operational amplifier with excellent input offset voltage performance, eg. LT1012.

Envelope Detection

When configured for envelope detection it is necessary to keep transmission-line lengths to a minimum and select external components with good RF performance to support wide bandwidth baseband signals.

With a bias-T, which can be as simple as a shunt resistor and a series capacitor connected to VDET, the bias current is regulated with the resistor while the envelope signal can pass the capacitor.

Input impedance at the pad of VDET is 200 Ohm. The reference output, VREF, is not required for envelope detection.

Temperature Sensor

A PN-diode temperature sensor with grounded cathode is available on-chip. Typical bias current is 100 uA and can be achieved by connecting eg. a 36.5k resistor between V_TEMP and a +5.0 V supply. Diode voltage is 1210 mV (typ.) at +25 °C and -1.4 mV/°C.

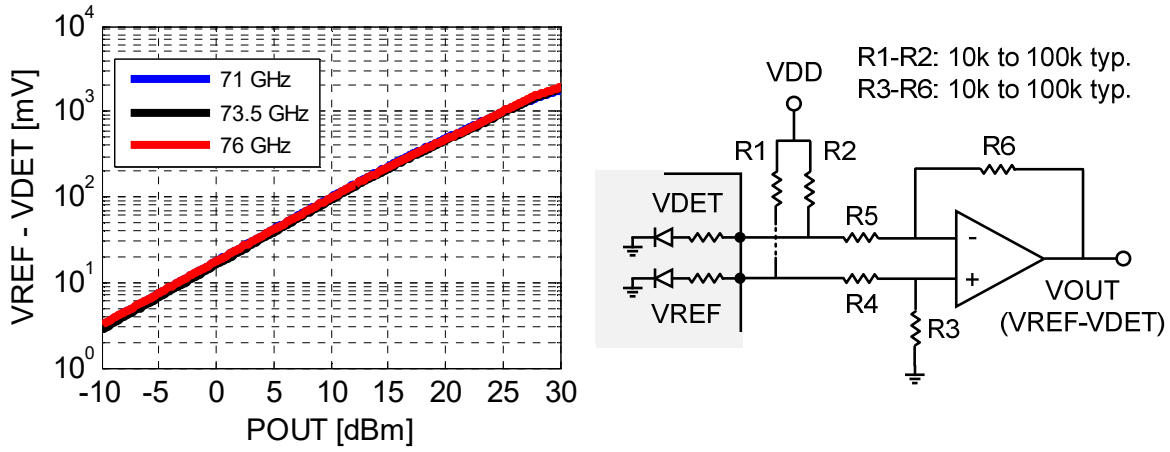

Figure 16. Detector output (left) and the external detector circuit (right)

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Assembly Diagram

Drains on side A are connected internally to the corresponding drains on side B. The circuit can be powered by connecting supplies to drains on A, B or both sides.

Always make sure that the rated maximum drain current is never exceeded. For high-power applications we therefore recommend connecting drain supplies to both A and B.

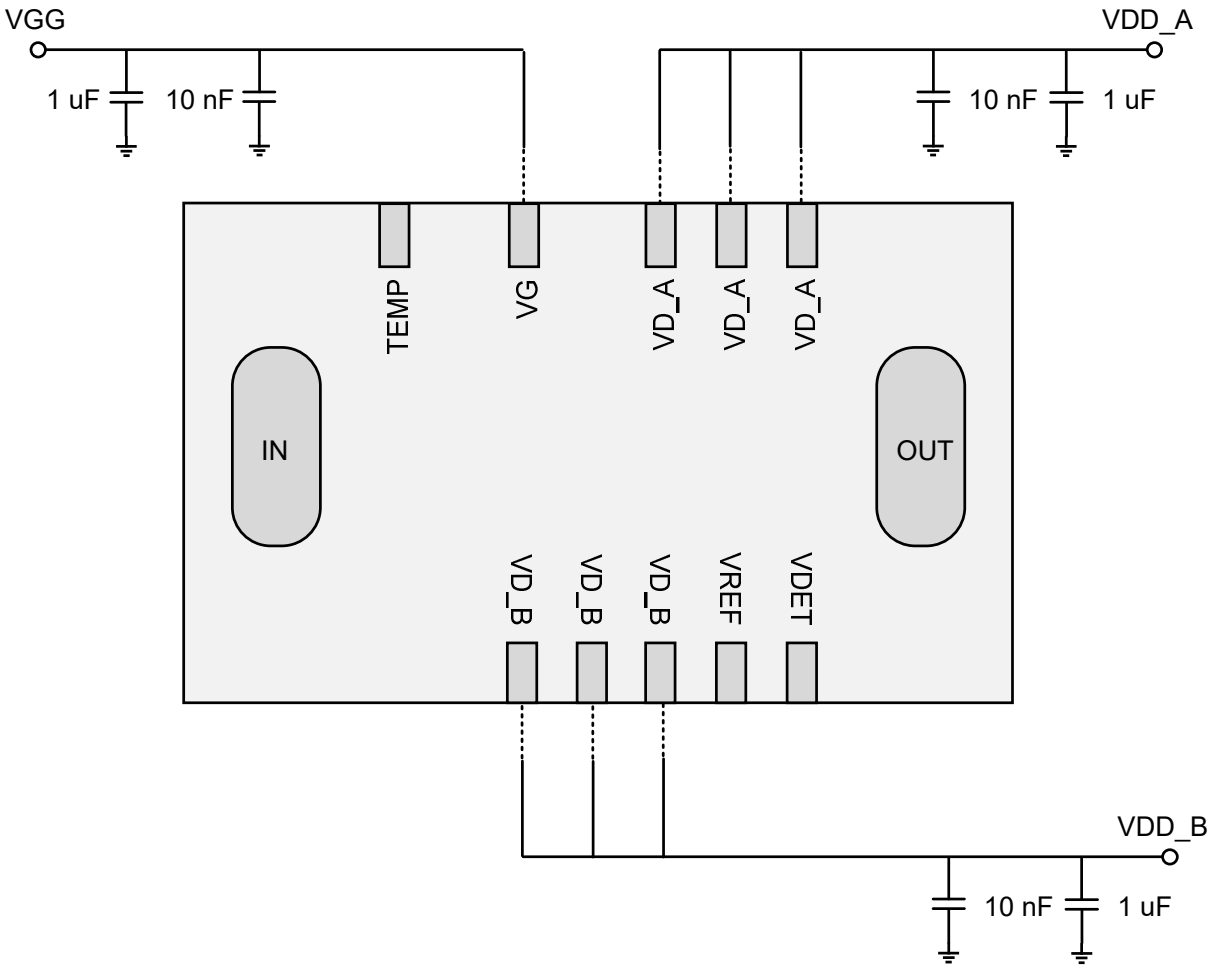

Figure 17. Assembly diagram

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Assembly Guidelines

Mount the package to an electrically grounded plane with excellent thermal properties. Make sure the surface is clean and flat before attaching the package.

DC Bypass

For stable operation locate external DC bypass capacitors near the package to reduce trace length and corresponding inductance. See assembly diagram for a recommended bypass network. Use low ESR ceramic or tantalum SMD capacitors.

Outline Drawing

Dimensions are in mm. The package hight is 4 mm. A dxf file is also available on request for use with CAD tools.

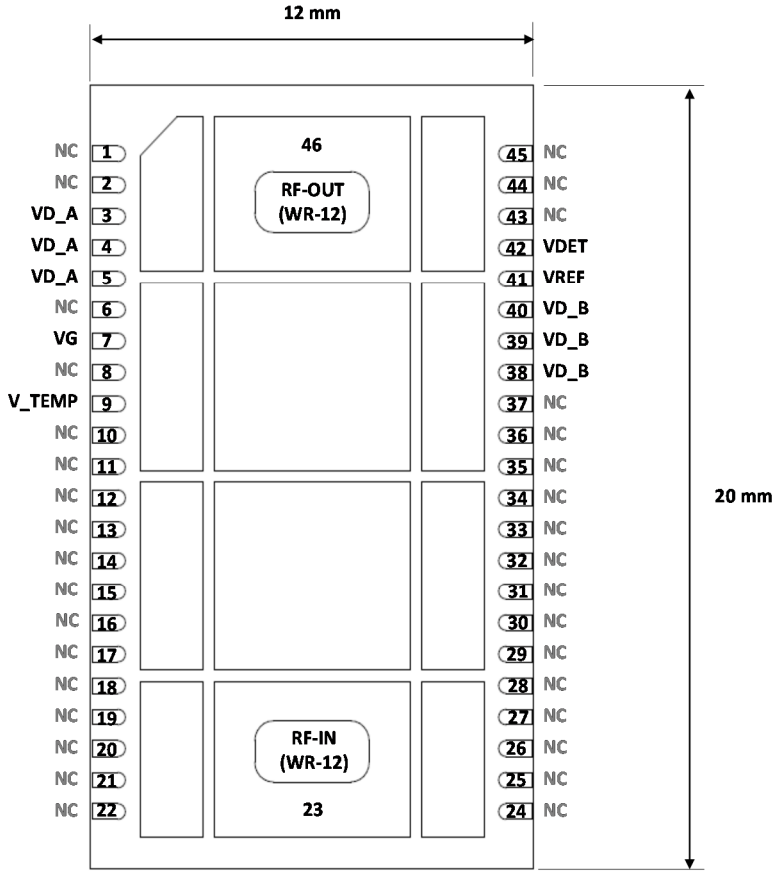

Figure 18. Package outline drawing

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