

## FEATURES

- SMD package (WR-10 interface)
- 92-96 GHz
- 27 dBm PSAT
- 12 dB gain
- Integrated detector
- Nominal bias: 4.0 V and 1.3 A
- Size: 12 x 15 x 4 mm

## APPLICATIONS

- Radar and imaging
- Point-to-point communication
- Instrumentation
- Fiber over radio

## DESCRIPTION

The gAPZ0095A is a GaAs pHEMT four-stage power amplifier in a surface mount package optimized for 92-96 GHz. It is ideal for high power W-band radar applications and long-range spectral efficient point-to-point communication.

At a nominal bias of 4.0 V and 1.3 A the MMIC dissipates 5.2 W and deliver 27 dBm saturated power at 6 % PAE.

A temperature compensated detector is available and can be configured for RMS power or envelope detection.

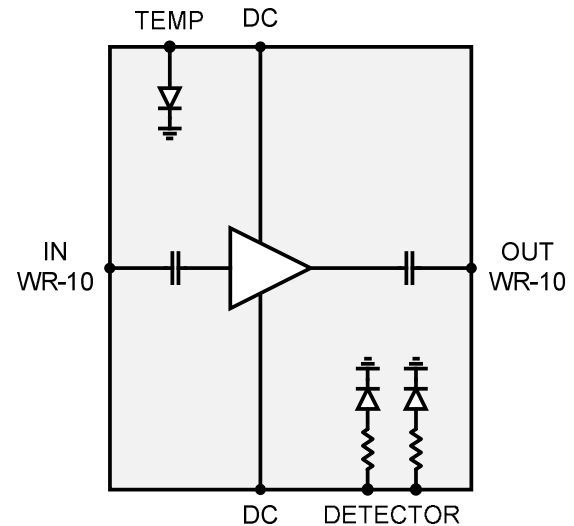


Figure 1. Circuit block diagram

## ELECTRICAL SPECIFICATIONS

**Table 1. Electrical specifications, backside temperature +25 °C, nominal bias**

Parameter	Min	Typ	Max	Unit
Frequency Range (performance)	92		96	GHz
Frequency Range (extended)	85		100	GHz
Gain		12		dB
Gain Temperature Slope		-0.05		dB/°C
OP1dB		TBD		dBm
PSAT (3 dB compression)		27		dBm
PAE at PSAT		6		%
OIP3		TBD		dBm
Input Return Loss		15		dB
Output Return Loss		15		dB
Detector Output at POUT (VREF - VDET)	-10 dBm		3	mV
	0 dBm		20	
	10 dBm		100	
	20 dBm		500	
	30 dBm		2000	
PDC (quiescent)	4.0 V / 1.3 A		5200	mW

**Table 2. Absolute maximum ratings**

Gate voltage (VG..)	-2.0 V
Drain voltage (VD..)	+4.5 V
Drain currents: VD_A or VD_B (one-sided bias) VD_A and VD_B (two-sided bias)	1560 mA 1720 mA
RF input power	+20 dBm
Junction temperature (1 million hours MTTF) Thermal resistance (+85 °C backside temp, incl. epoxy)	+150 °C 10 °C/W
Operating temperature	-40 to +85 °C
Storage temperature	-65 to +150 °C

## PIN CONFIGURATION AND BIAS

Always apply the gate supplies first followed by the drain supplies.

It is recommended to initially set the gate to -1.6 V and adjust the gate supply to achieve the specified total drain current of 1.3 A.

The typical gate voltage can vary by up to 0.2 V from what is noted.

The drain currents are listed with all RF input signals off.

**Table 3. Pin configuration**

Pad No.	Reference	Supply (V)	Current (mA)	Function
1-2	NC			
3-5	VD_A	4.0	650	Bias
6	NC			
7	VG_A	-0.5 (typ.)		Bias
8	NC			
9	V_TEMP	See temperature sensor		Temperature output
10-16	NC			
17	RF IN	WR-10		RF input
18-23	NC			
24	VG_B	-0.5 (typ.)		Bias
25	NC			
26-28	VD_B	4.0	650	Bias
29	VREF	See detector operation		Detector reference
30	VDET			Detector output
31-33	NC			
34	RF OUT	WR-10		RF output

## TYPICAL PERFORMANCE

Unless otherwise noted, all data presented has been obtained with a test-fixture, at room temperature and at nominal bias.

The two-tone RF input signal at -8 dBm/tone has a separation frequency of 50 MHz.

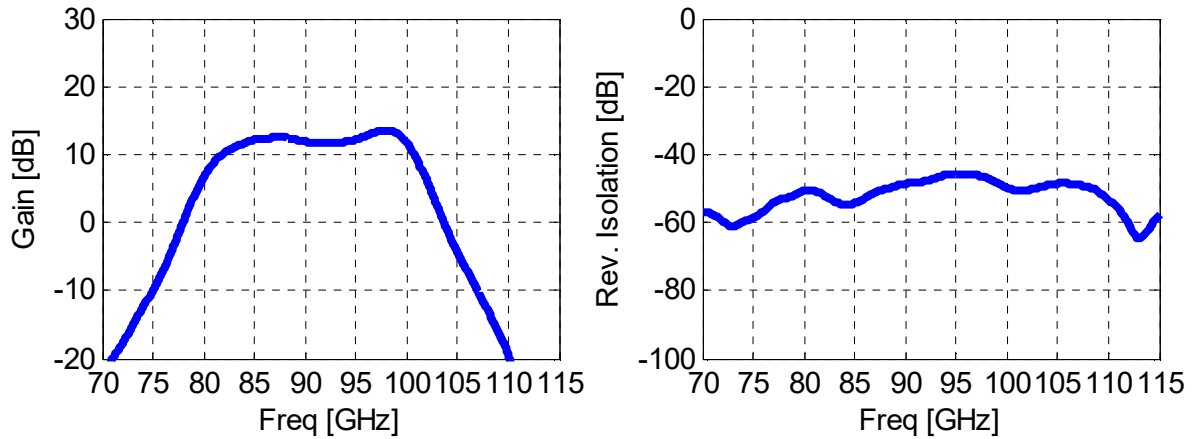


Figure 2. Gain (left) and reverse isolation (right)

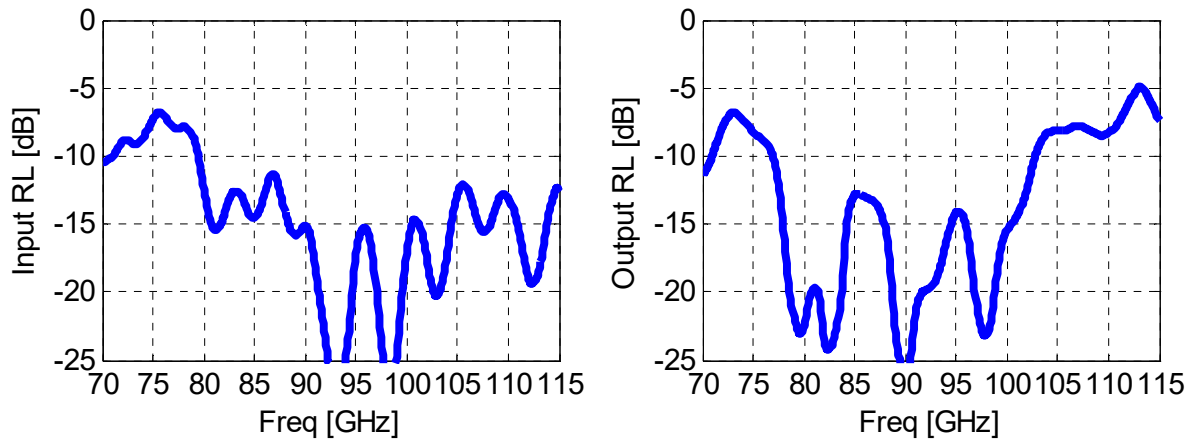


Figure 3. Input (left) and output return loss (right)

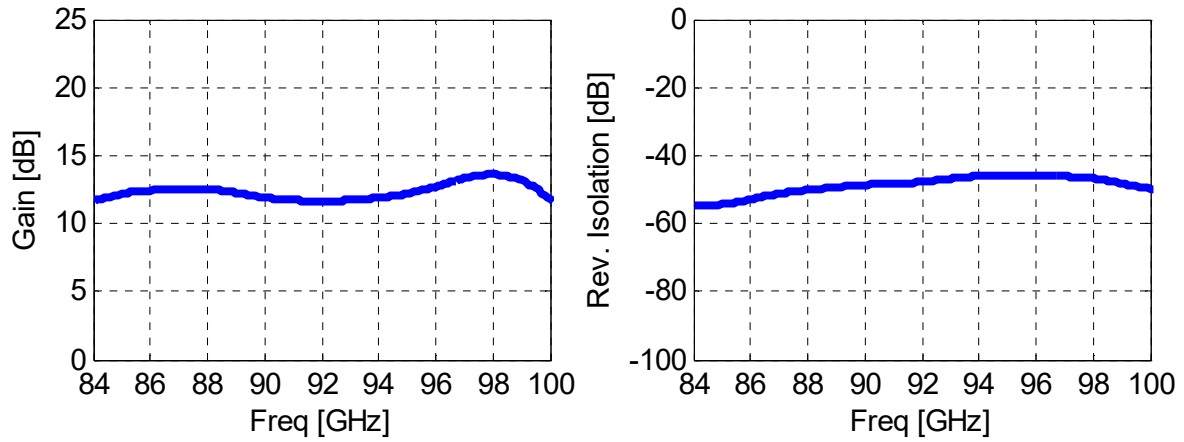


Figure 4. In-band gain (left) and reverse isolation (right)

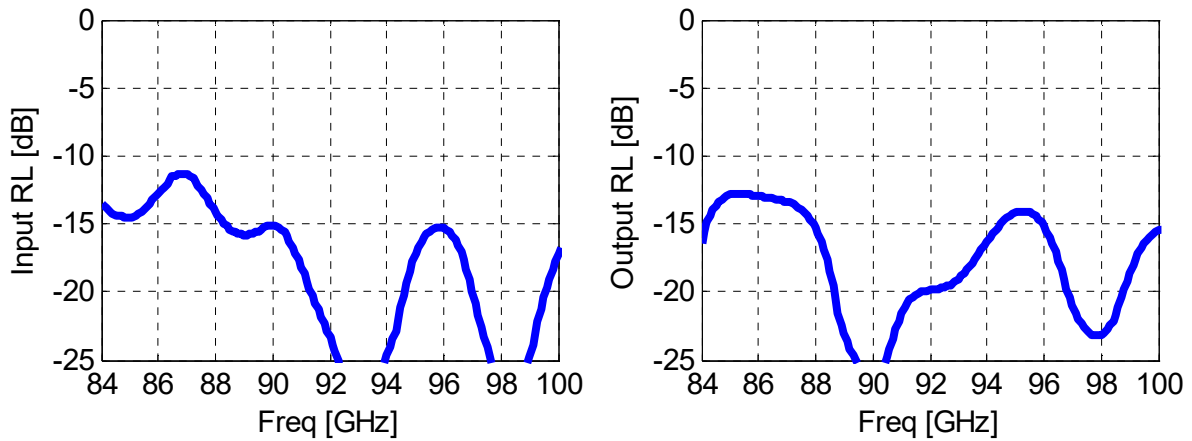


Figure 5. In-band input (left) and output return loss (right)

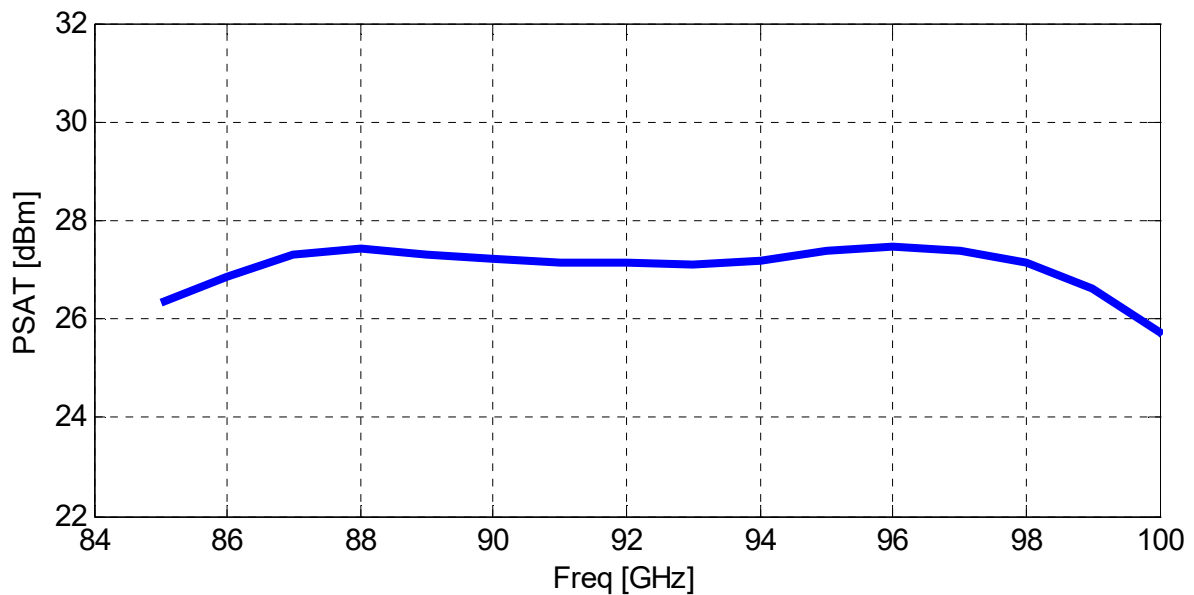


Figure 6. PSAT

## DETECTOR OPERATION

The detector can be configured for RMS power or envelope detection. Leave VREF and VDET as no-connect if not used.

To compensate for thermal variation, a reference is included on chip. Therefore, to get a temperature compensated output, take the difference of VREF and VDET using the recommended external detector circuit. Detector bias is applied through VDD and a pair of resistors (R1 and R2), ideally with close to identical values, typically 10k to 100k. We recommend selecting an operational amplifier with excellent input offset voltage performance, eg. LT1012.

## ENVELOPE DETECTION

When configured for envelope detection it is necessary to keep transmission-line lengths to a minimum and select external components with

good RF performance to support wide bandwidth baseband signals.

With a bias-T, which can be as simple as a shunt resistor and a series capacitor connected to VDET, the bias current is regulated with the resistor while the envelope signal can pass the capacitor. Typical bias current is 1 mA.

Input impedance at the pad of VDET is 200 Ohm. The reference output, VREF, is not required for envelope detection.

## TEMPERATURE SENSOR

A PN-diode temperature sensor with grounded cathode is available on-chip. Typical bias current is 100 uA and can be achieved by connecting eg. a 36.5k resistor between V\_TEMP and a +5.0 V supply. Diode voltage is 1210 mV (typ.) at +25 °C and -1.4 mV/°C.

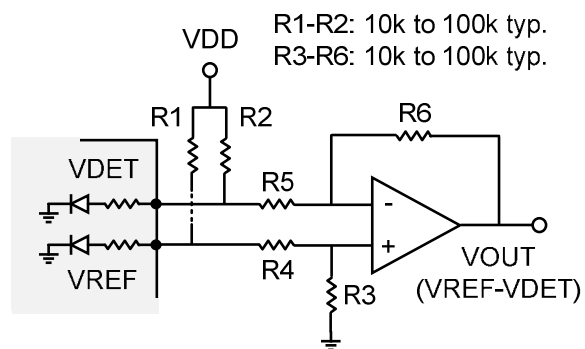
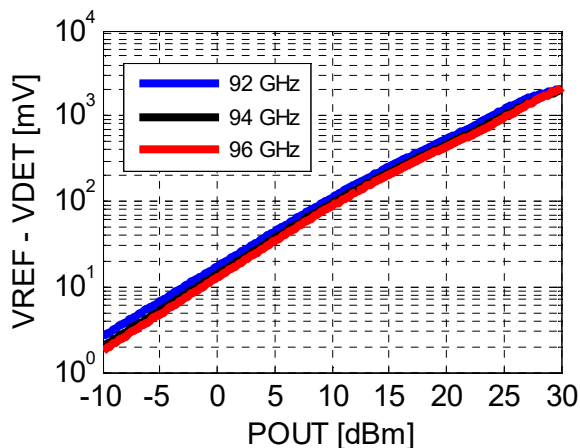


Figure 7. Detector output (left) and the external detector circuit (right)

### ASSEMBLY DIAGRAM

Gates and drains on side A are connected internally to the corresponding gates and drains on side B. The circuit can be powered by connecting supplies to drains on A, B or both sides and

similarly the same applies for gates. Always make sure that the rated maximum drain current is never exceeded. For high-power applications we therefore recommend connecting drain supplies to both A and B.

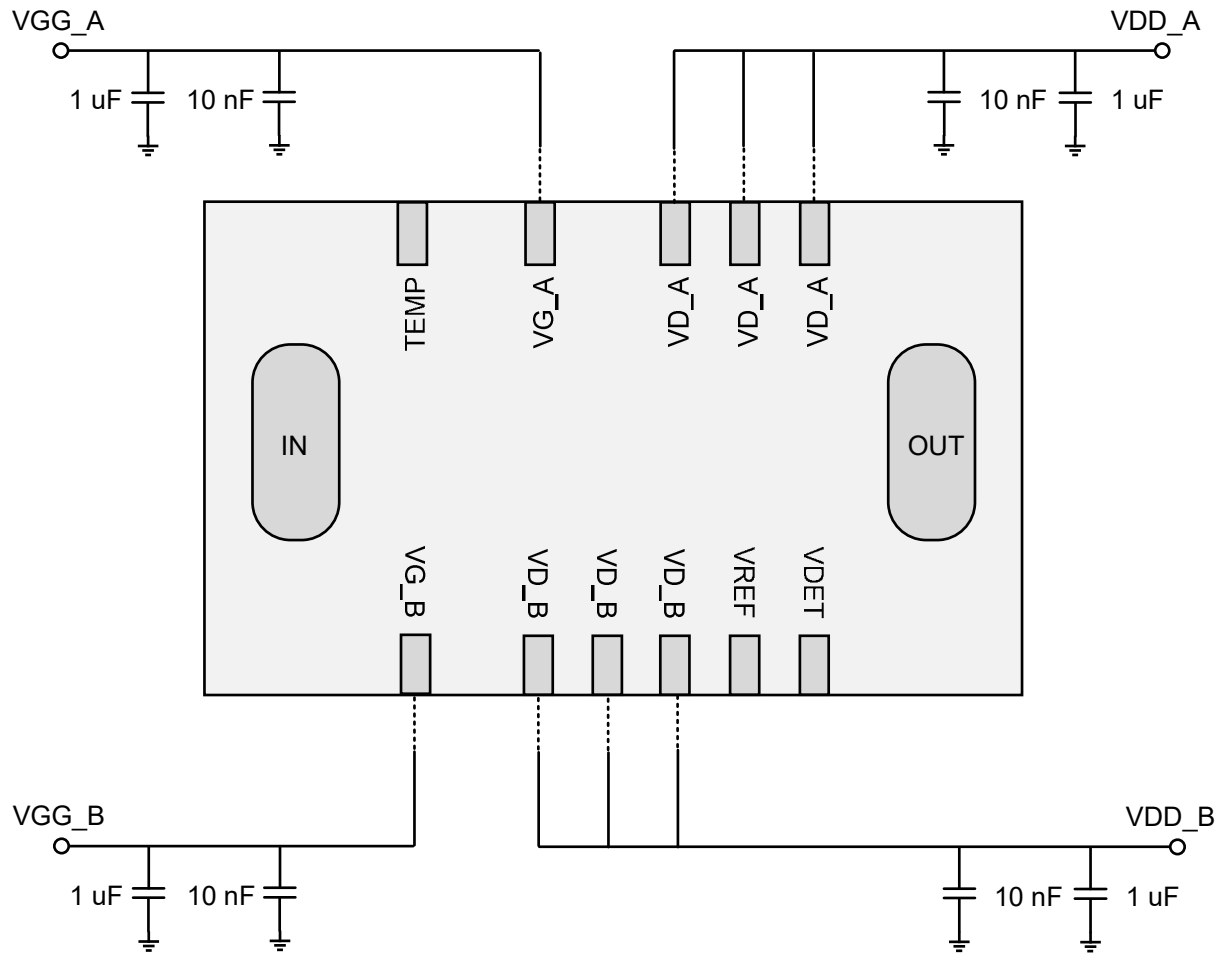


Figure 8. Assembly diagram

## ASSEMBLY GUIDELINES

Mount the package to an electrically grounded plane with excellent thermal properties. Make sure the surface is clean and flat before attaching the package.

## DC BYPASS

For stable operation locate external DC bypass capacitors near the package to reduce trace

length and corresponding inductance. See assembly diagram for a recommended bypass network. Use low ESR ceramic or tantalum SMD capacitors.

## OUTLINE DRAWING

Dimensions are in mm. The package height is 4 mm. A dxf file is also available on request for use with CAD tools.

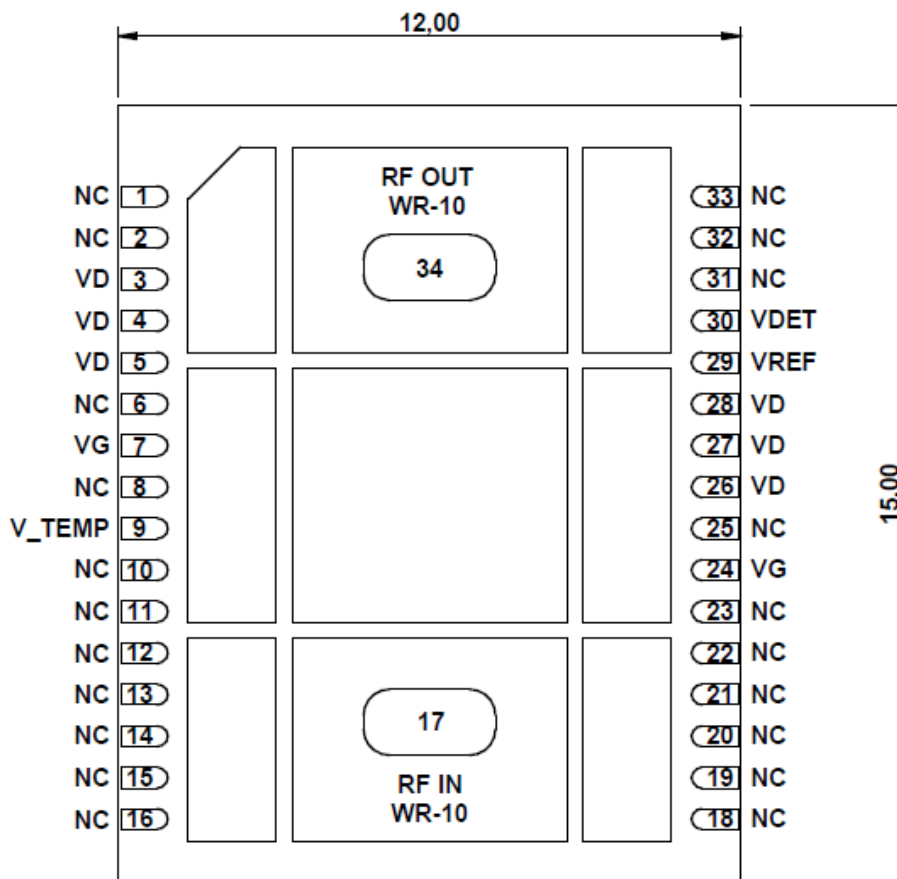


Figure 9. Package outline drawing